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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/790,205	03/02/2004	Jia-Pei Shen	95-528	1032

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MANELLI DENISON & SELTER
2000 M STREET NW SUITE 700
WASHINGTON, DC 20036-3307

EXAMINER	
DO, CHAT C	
ART UNIT	PAPER NUMBER
2193	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	03/28/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No.	Applicant(s)	
	10/790,205	SHEN ET AL.	
	Examiner	Art Unit	
	Chat C. Do	2193	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *03/02/04; 04/21/04; 03/07/05; 10/12/06*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-12* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-12* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *21 April 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *04/21/04; 10/12/06*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 101

1. 35 U.S.C. 101 reads as follows:

> Whoever invents or discovers any new and useful process, machine, manufacture, or composition of matter, or any new and useful improvement thereof, may obtain a patent therefor, subject to the conditions and requirements of this title.

2. Claims 1-12 are rejected under 35 U.S.C. 101 because the claimed invention is directed to non-statutory subject matter.

Claims 1-12 cite a method and circuit for performing FFT in accordance with a predetermined mathematical algorithm. In order for claims to be statutory, claims must either include a practical/physical application or a concrete, useful, and tangible result. However, claims 1-12 merely disclose steps/components for performing FFT in circuit without further disclosing a practical/physical application or a useful and tangible result. Therefore, claims 1-12 are directed to non-statutory subject matter.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

4. Claims 1-12 are rejected under 35 U.S.C. 102(e) as being anticipated by Ryu (U.S. 7,007,056).

Re claim 1, Ryu discloses in Figures 4-7 a method in a Fast Fourier Transform (FFT) circuit having at least a Radix-4 butterfly element (e.g. abstract and Figure 4 with calculation unit 560 and col. 8 lines 5-8), the method including: storing first and second equal portions of a prescribed number of data values (e.g. input in Figure 4 is the input data which are divided and input equally into the memories 510 and 520) in first and second memory portions (e.g. memories 510 and 520 in Figure 4), respectively, according to a prescribed mapping that ensures the first and second memory portions are accessed for each in-place computation operation (e.g. col. 3 lines 5-22 and Figure 6); executing a prescribed number of FFT stages each having a prescribed number of the in-place computation operations relative to the prescribed number of data values, wherein the executing step includes performing each in-place computation operation (e.g. Figure 6 and butterfly calculation unit 560 in Figure 4 for looping computing butterfly for all input data; typical calculation of 8-points FFT is seen in Figure 3): (1) concurrently accessing an equal number of stored data values from the first memory portion and the second memory portion (e.g. abstract, col. 4 lines 14-32, and col. 3 lines 5-12); and (2) supplying the accessed data values to the at least Radix-4 butterfly element for calculation of respective calculation results (e.g. computed by the butterfly calculation unit 560 in Figure 4 and col. 8 lines 5-8).

Re claim 2, Ryu further discloses in Figures 4-7 the step of performing each in-place computation includes storing the calculation results in the first memory portion and

the second memory portions at memory locations having stored the respective accessed data values (e.g. col. 3 lines 5-22 and col. 6 lines 6-13).

Re claim 3, Ryu further discloses in Figures 4-7 the first and second memory portions each are dual-port memory devices (e.g. each of memories 510 and 520 has its own input and output port as read and write port respectively in Figure 4), the executing step including accessing the stored data values for a subsequent one of the in-place computation operations concurrently during the storing of the calculation results for each in-place computation operation (e.g. col. 3 lines 5-22 and col. 6 lines 6-13).

Re claim 4, Ryu further discloses in Figures 4-7 the executing step includes performing the in-place computation operations for a first of the FFT stages in a prescribed order based on an input sequence of one of the in-place operations for a second of the FFT stages (e.g. col. 3 lines 5-22, col. 6 lines 6-13).

Re claim 5, Ryu further discloses in Figures 4-7 the executing step further includes initiating the one in-place operation for the second of the FFT stages after having completed the prescribed order of the in-place computation operations relative to the input sequence (e.g. Figures 3 and 6, and col. 8 lines 1-4).

Re claim 6, Ryu further discloses in Figures 4-7 the concurrently accessing step includes accessing, for each clock cycle (e.g. col. 8 lines 1-4), a corresponding stored data value from a read port of the first memory portion and a corresponding stored data value from a read port of the second memory portion, the storing step including writing, during each clock cycle (e.g. col. 8 lines 1-4), a corresponding calculation result via a

write port of the first memory portion and a corresponding calculation result via a write port of the second memory portion (e.g. col. 5 line 44 to col. 7 line 28).

Re claim 7, it is a circuit claim of claim 1. Thus, claim 7 is also rejected under the same rationale as cited in the rejection of rejected claim 1.

Re claim 8, it is a circuit claim of claim 2. Thus, claim 8 is also rejected under the same rationale as cited in the rejection of rejected claim 2.

Re claim 9, it is a circuit claim of claim 3. Thus, claim 9 is also rejected under the same rationale as cited in the rejection of rejected claim 3.

Re claim 10, it is a circuit claim of claim 4. Thus, claim 10 is also rejected under the same rationale as cited in the rejection of rejected claim 4.

Re claim 11, it is a circuit claim of claim 5. Thus, claim 11 is also rejected under the same rationale as cited in the rejection of rejected claim 5.

Re claim 12, it is a circuit claim of claim 6. Thus, claim 12 is also rejected under the same rationale as cited in the rejection of rejected claim 6.

Conclusion

5. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

a. U.S. Patent Publication No. 2005/0102342 to Greene discloses methods and apparatus for FFT.

b. U.S. Patent Publication No.2004/0243656 to Sung et al. disclose a digital signal processor structure for performing length-scalable FFT.

c. U.S. Patent No. 7,164,723 to Sunwoo discloses a modulation apparatus using mixed-radix FFT.

d. U.S. Patent No. 6,609,140 to Greene discloses methods and apparatus for FFT.

e. U.S. Patent No. 6,356,926 to Andre discloses a device and method for calculating FFT.

f. U.S. Patent No. 3,673,399 to Hancke et al. disclose a FFT processor with unique addressing.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Chat C. Do whose telephone number is (571) 272-3721. The examiner can normally be reached on M => F from 7:00 AM to 5:30 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Meng-Ai An can be reached on (571) 272-3756. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Chat C. Do
Examiner
Art Unit 2193

March 23, 2007